Energy Efficiency Scaling for Two Decades (EES2) R&D Roadmap — Public Feedback

DATE: August 14, 2024
SUBJECT: DE-FOA-0003426: Request for Information (RFI)

Description

This is a Request for Information (RFI) issued by the U.S. Department of Energy (DOE) on behalf of the Advanced Materials and Manufacturing Technologies Office (AMMTO). The intent of this RFI is to solicit feedback from affected stakeholders on the Energy Efficiency Scaling for Two Decades (EES2) Initiative in general and on the draft EES2 Research and Development (R&D) Roadmap that accompanies this RFI.

Background

The mission of DOE is to ensure America's security and prosperity by addressing its energy, environmental, and nuclear challenges through transformative science and technology solutions.[1] AMMTO's mission is to inspire people and accelerate innovation to transform materials and manufacturing for America's energy future. AMMTO programs support research, development, and demonstration of next-generation materials and innovative manufacturing technologies to increase U.S. industrial competitiveness and to drive economy-wide decarbonization.

The integrated circuits or "chips" made by the semiconductor industry are essential to microelectronics and to the modern economy. The microelectronics industry is currently facing the dual challenges of more sluggish energy efficiency gains and emerging sources of fast-growing energy demand for computing. For decades, the miniaturization of transistors reliably doubled the energy efficiency of chips every two years, but this biennial energy efficiency doubling began to slow around 2005. With new sources of energy demand emerging, such as energy-intensive AI applications, energy use in key microelectronics applications in the information technology (IT) sector is on an unsustainable growth trajectory. For example, today's exponentially increasing use computing is causing explosive growth in the electricity needed for both operation and cooling of existing and future planned data centers.

The challenge of microelectronics energy efficiency is also a supply chain security and national security challenge. It is now critical to strengthen the IT manufacturing sector, which includes

[1] U.S. Department of Energy, "Mission," https://www.energy.gov/mission, accessed 2024.

computing, communications, and other applications of the nearly trillion-dollar global semiconductor and microelectronics manufacturing enterprise. Building technological leadership by manufacturing far more energy efficient products is also critical so that the industry becomes more resilient, technologically cutting-edge, and less dependent on continuing government incentives.

Recognizing the pivotal role of microelectronics in the global economy and the importance of addressing the industry's energy trends, DOE announced an R&D roadmapping effort to reach 1000x energy efficiency in twenty years. DOE then launched the Energy Efficiency Scaling for Two Decades (EES2) initiative in 2022, one month after the CHIPS and Science Act was signed into law. EES2 is a partnership with industry, academia, and national labs that provide microelectronics stakeholders an opportunity to collaborate with AMMTO on outreach and a strategy to achieve energy efficiency scaling: doubling microelectronics' energy efficiency every two years until a net efficiency increase of 1,000x is achieved in twenty years or faster. DOE and the sixty-five organizations that to date have signed the EES2 pledge believe that getting back to pre-2005 levels of efficiency improvement—biennially doubling energy efficiency—is necessary for public benefit and to ensure technological leadership.

In addition to participating in the development of the attached R&D roadmap, the EES2 pledge's commitments also include, but are not limited to:

a. Documenting and learning from microelectronics' past and forecasted future ability to enable all sectors of the economy to become more energy efficient and sustainable.
b. Identifying and publicizing the problems solved and the opportunities offered by microelectronics' Energy Efficiency Scaling over 2 Decades (EES2).
c. Exploring formation of a partnership, perhaps named "EES2 Allies," that enables the EES2 1,000x efficiency goal by leading future EES2 R&D roadmapping efforts after 2025. The partnership would catalyze the deployment of cost-effective technologies needed to continue doubling microelectronics' energy efficiency every two years.

The EES2 pledge also asserts that working to achieve ambitious microelectronics energy efficiency goals is urgently needed and is a pathway to technological leadership.

While the EES2 pledge is about life-cycle energy efficiency, this first version of the EES2 roadmap focuses on reductions in the energy use phase of computing and the "compute stack" and is guided by previous DOE work recommending co-design across adjacent layers of this stack. Therefore, the roadmap team was divided into eight specialized working groups, each focusing on two adjacent layers of the computing stack or on enabling technologies and approaches. Working group deliberations focused on identifying key emerging energy efficient

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technologies and their challenges and solutions. The EES2 working groups for version 1.0 are:

a. Materials and Devices (MnD)
b. Circuits and Architectures (CnA)
c. Advanced Packaging and Heterogenous Integration (APHI)
d. Algorithms and Software (AnS)
e. Power and Control Electronics (PaCE)
f. Manufacturing Energy Efficiency and Sustainability (MEES)
g. Metrology and Benchmarking (MnB)
h. Education and Workforce Development (EWD)

This roadmap does not cover every aspect of energy efficiency in microelectronics and its applications. This version 1.0 roadmap identifies 55 candidate "technologies to beat" that were identified by working groups comprising paired elements of the compute stack. As the EES2 team continues to focus on accelerating and expanding efficiency efforts, future versions will likely incorporate emerging technologies such as quantum computing, nature-inspired architectures, and optoelectronics. Future versions will also likely focus on avoiding other potential electricity use surges due to non-compute applications such as 6G+ communication technologies. The goal is to put microelectronics energy use back on a sustainable path over the next 20 years with continuing updates of the EES2 roadmap that respond to technological advancements and changes in demand.

Purpose

The purpose of this RFI is to solicit feedback from industry, academia, research laboratories, government agencies, and other stakeholders on issues related to energy efficiency in microelectronics and its applications, particularly computing applications. EERE is specifically interested in feedback on the initial version (1.0) of the EES2 technology roadmap that accompanies this RFI. Feedback on other aspects of EES2 also are invited.

Disclaimer and Important Notes

This RFI is not a Funding Opportunity Announcement (FOA); therefore, EERE is not accepting applications at this time. EERE may issue a FOA in the future based on or related to the content and responses to this RFI. However, EERE may also elect not to issue a FOA. There is no guarantee that a FOA will be issued as a result of this RFI. Responding to this RFI does not provide any advantage or disadvantage to potential applicants if EERE chooses to issue a FOA regarding the subject matter. Final details, including the anticipated award size, quantity, and timing of EERE funded awards, will be subject to Congressional appropriations and direction.

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Any information obtained as a result of this RFI is intended to be used by the Government on a non-attribution basis for planning and strategy development; this RFI does not constitute a formal solicitation for proposals or abstracts. Your response to this notice will be treated as information only. EERE will review and consider all responses in its formulation of program strategies for the identified materials of interest that are the subject of this request. EERE will not provide reimbursement for costs incurred in responding to this RFI. Respondents are advised that EERE is under no obligation to acknowledge receipt of the information received or provide feedback to respondents with respect to any information submitted under this RFI. Responses to this RFI do not bind EERE to any further actions related to this topic.

Confidential Business Information

Pursuant to 10 CFR 1004.11, any person submitting information that he or she believes to be confidential and exempt by law from public disclosure should submit via email, postal mail, or hand delivery two well-marked copies: one copy of the document marked "confidential" including all the information believed to be confidential, and one copy of the document marked "non-confidential" with the information believed to be confidential deleted. Submit these documents via email or on a flash drive, if feasible. DOE will make its own determination about the confidential status of the information and treat it according to its determination.

Evaluation and Administration by Federal and Non-Federal Personnel

Federal employees are subject to the non-disclosure requirements of a criminal statute, the Trade Secrets Act, 18 USC 1905. The Government may seek the advice of qualified non-Federal personnel. The Government may also use non-Federal personnel to conduct routine, nondiscretionary administrative activities. The respondents, by submitting their response, consent to EERE providing their response to non-Federal parties. Non-Federal parties given access to responses must be subject to an appropriate obligation of confidentiality prior to being given access. Submissions may be reviewed by support contractors and private consultants.

Request for Information Categories and Questions

Category A: Commentary about the EES2 initiative goals and objectives

Question A-1: Is the target of returning to biennial efficiency doubling and doing so for 20 years appropriate, too ambitious, or not ambitious enough? What changes might improve it?

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Question A-2: Are cooperative and accelerated research, development, and demonstration the best way to reach the EES2 goals? What are other ways the EES2 Initiative partners might cooperate to reach the goals?
Question A-3: How does the EES2 R&D roadmap's focus specifically on technologies for energy efficiency compare with other semiconductor industry R&D roadmaps currently available or in development?
Question A-4: What types of interim goals and time horizons should DOE consider to achieve a 1,000x efficiency increase in microelectronics?
Question A-5: What is the most effective way for the EES2 partnership to measure progress toward its goals and assess the energy footprint of microelectronics over time at multiple scales? Should this be achieved through a new type of technology efficiency survey with reference benchmarks? What other methods might the partnership consider?

Category B: Commentary about the roadmap document

B.1 Overall Report Structure/Content

Question B.1-1: Is the structure of the roadmap effective in distinguishing between compute stack and enablers?
Question B.1-2: Is the content of each chapter appropriately aligned with its title and the overall goals of the roadmap?
Question B.1-3: Is the overall content accessible and detailed enough for high level policy makers?
Question B.1-4: What additional analyses related to energy efficiency should the team consider incorporating into the roadmap and other EES2 efforts?

B.2 Introduction

Question B.2-1: Have the motivation and the scope of the problem been adequately and accurately framed? If not, please provide suggestions for how these can be improved.
Question B.2-2: Does the document comprehensively explain other related work? Please indicate if any pertinent related works have been omitted.
Question B.2-3: Has sufficient background information been provided to enable stakeholders to fully understand the report?

B.3 Technologies for the Compute Stack

Question B.3-1: Has the energy saving potential of any of the identified stack technologies been overstated or understated? If so, please explain in detail.
Question B.3-2: Are any topics in this section presented incompletely or inaccurately? If so, please provide specific recommendations.

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Question B.3-3: Are the interrelationships and potential for co-design between the proposed technologies clearly demonstrated?

Question B.3-4: Are there any promising compute stack technologies that could significantly contribute to the EES2 goals but have been overlooked? If so, please detail these technologies, including their current and anticipated energy consumption, key challenges, and potential solutions. Note that several technologies are already planned for inclusion in version 2.0. Please provide references to support your suggestions.

Question B.3-5: If able, please provide insights on the current advancements, energy efficiency impacts, and integration challenges of cryogenic low temperature complementary metal-oxide-semiconductors (CMOS), specifically those operating at temperatures from 77–150 Kelvin. Include references to recent studies or data supporting their potential inclusion in our energy efficiency roadmap. What are the anticipated development trajectories and scalability issues for these technologies?

B.4 Enablers

Question B.4-1: Has the energy saving potential of any of the identified technologies been overstated or understated? If so, please explain in detail.

Question B.4-2: Are any specific topics in this section presented incompletely or inaccurately? If so, please provide specific recommendations.

Question B.4-3: Have any technology candidates with significant potential to contribute to the EES2 goals been omitted? If so, please detail these technologies, including their current and anticipated energy consumption, key challenges, and potential solutions. Please also provide references to support your suggestions.

Question B.4-4: Have any education and workforce development measures with significant potential to contribute to the EES2 goals been omitted? If so, please explain in detail, and identify major challenges, solutions, and actions needed to implement the measure. Include references as appropriate to support inclusion of this measure.

Question B.4-5: If possible, please provide insights on the current advancements, energy efficiency impacts, and integration challenges of high temperature superconductors in data center power applications. What are the anticipated development trajectories and scalability issues for these technologies? Include references to recent studies or data supporting their potential inclusion in the EES2 roadmap.

B.5 Conclusion

Question B.5-1. Has this section adequately and accurately synthesized the results and implications of the preceding chapters? If not, please provide suggestions for how this section can be improved.

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Category C: Commentary about the process and future steps

Question C-1: Do you have suggestions for how to improve the plans for future work outlined in the conclusion?

Question C-2: Are there specific funding initiatives that DOE should undertake to further the EES2 objectives?

Question C-3: What other stakeholders should EES2 collaborate with to maximize the impact on energy efficiency, and should these additional collaborators participate only in the roadmap or in all EES2 activities (e.g., analysis, outreach)?

Request for Information Response Guidelines

Responses to this RFI must be submitted electronically to micro.electronics@ee.doe.gov no later than 5:00pm (EDT) on December 16th, 2024. Responses must be provided as a Microsoft Word (.docx) attachment to an email. Since a marked up copy of the roadmap Word document will exceed 25 MB, it is recommended that you compress (i.e., zip) the file, along with any separate comments you have, to ensure message delivery.

Please identify your answers by responding to a specific question or topic if applicable. Respondents may answer as many or as few questions as they wish.

There is no specific page limit for the response. Please do not include generic company background information or any other content not directly related to the questions. Respondents are encouraged to make detailed suggested edits and comments within the body of the roadmap document in “track changes” mode and provide the marked-up document as an attachment to their response email.

EERE will not respond to individual submissions or publish publicly a compendium of responses. A response to this RFI will not be viewed as a binding commitment to develop or pursue the project or ideas discussed.

Respondents are requested to provide the following information at the start of their response to this RFI:

- Company/institution name.
- Company/institution contact.
- Contact's address, phone number, and e-mail address.

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